

HM07105 High Efficiency DC/DC Module

FEATURES

- Complete Switch Mode Power Supply
- Wide Input Voltage Range from +1.8V to 25V
- 7A DC Output Current
- Adjustable +0.5V to + 5V Output Range
- Constant On-time Control for Fast Transient Response
- Power Saving Mode Option
- Enable Function Option
- Power Good Indicator
- Internal Digital Soft-Start
- Output Over-Voltage Protection
- Output Under-Voltage Protection
- Over-Current Protection by Low-side MOSFET $R_{DS(ON)}$ Sensing
- Over-Temperature Protection
- Pb-Free RoHS Compliant Package
- Small Footprint, Low Profile Surface Mount Hybrid Package (15mm×15mm×3.5mm)

APPLICATIONS

- Notebook PC / UMPC
- Servers
- Industrial PC Equipment
- Point of Load Regulation
- Other General Purpose Step Down DC/DC
- PCI Express Graphical Processing Unit

DESCRIPTION

The HM07105 is a complete 7A, DC/DC step down power supply. Included in the package has the PWM controller, power MOSFETs, inductor, and most of support components. Operating over an input voltage range of 1.8V to 25V and supports an output voltage range of 0.5V to 5V that set by single dividing resistor. The high efficiency design delivers 7A continuous current. Only bulk input, output capacitors and few parameter setting components are needed to finish the design.

The HM07105 uses constant on-time control with extremely minimum on-time better for transient response. The HM07105 has internal soft-start, current limit, over voltage protection, under voltage protection, power good output and soft discharge upon shutdown. The HM07105 can be configured to operate power saving mode or not. At light loads, power saving mode enables the PWM controller to skip PWM pulses for better efficiency. The HM07105 has been set initial frequency and current limit for normally application which easy to design for power converter.

The low profile package (3.5mm) enables utilization of unused space on the bottom of PC boards for highly density point of load regulation. The HM07105 is packaged in a thermally enhanced, compact (15mm×15mm) and low profile (3.5mm) over-molded Hybrid Package Modular suitable for automated assembly by standard surface mount equipment. The HM07105 is Pb-free and RoHS compliance.

SIMPLIFIED BLOCK DIAGRAM

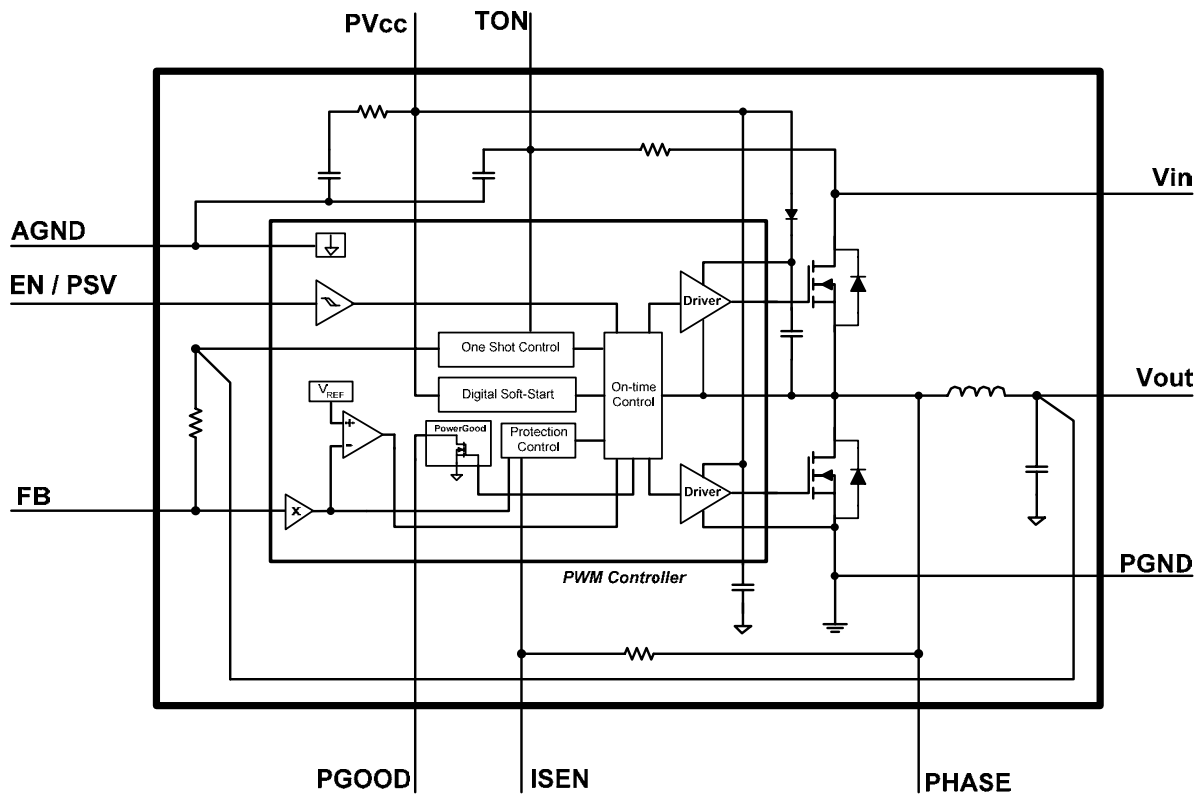
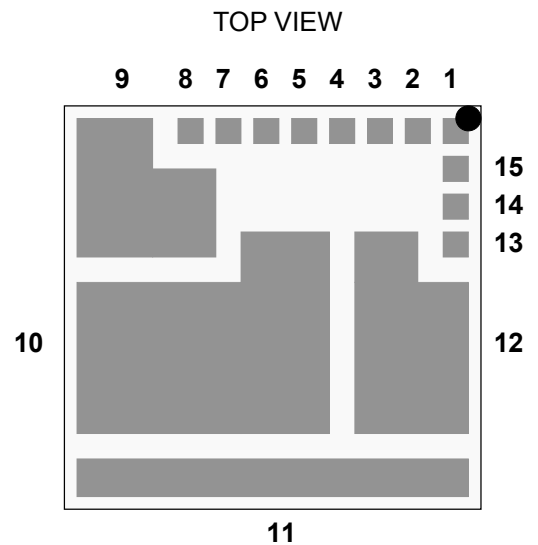


Figure 1. Internal Block Diagram

PACKAGE INFORMATION

Table 1. Pin Description

Pin	Symbol	Description
1	AGND	Analog ground
2	AGND	Analog ground
3	AGND	Analog ground
4	AGND	Analog ground
5	PVCC	Supply voltage
6	PVCC	Supply voltage
7	ISEN	Over current protection
8	TON	On-time and switching frequency setting
9	VIN	Power input
10	PHASE	Phase node
11	PGND	Power ground
12	VOUT	Power output
13	EN / PSV	Enable / Power saving mode input
14	FB	Feedback input
15	PGOOD	Power good signal output



HM07105 HYBRID MODULAR
(15mm x 15mm x 3.5mm)

ORDERING INFORMATION

PART NUMBER	PACKAGE
HM07105	Hybrid Package (15mm × 15mm × 3.5mm)

ABSOLUTE MAXIMUM RATINGS

Symbol	Limits	Unit
TON to AGND	-0.3 to +25	V
PVCC , EN / PSV, FB, PGOOD, Vo, ISEN to AGND	-0.3 to +6	V
PGND to AGND	-0.3 to +0.3	V
Phase to PGND	-1.2 ~ 30 (Note 1)	V
Vin to Phase	-1.2 ~ 30 (Note 1)	V
Tc	110	°C
Tstg	-40 to +125	°C

CAUTION : Stress over "Absolute Maximum Ratings" may cause permanent damage

RECOMMENDED OPERATING RATINGS

Symbol	Parameter	Limits	Unit
Vin	Input supply voltage	+1.8 to +25	V
Vout	Output voltage	+0.5 to +5	V
Ta	Ambient temperature range	-40 to +85	°C

THERMAL RESISTANCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Rth(j-a)	Thermal resistance from junction to ambient	Note 2	-	12.92	-	°C/W
Rth(j-c)	Thermal resistance from junction to case	Note 2 (Refer to Figure 11)	-	0.96	-	°C/W

Note 1 : V_{DS} (Drain to Source) specification for internal high-side and low-side MOSFET.

Note 2 : Rth(j-a) and Rth(j-c) are measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 114.5mm×101.5mm×1.6mm with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL CHARATERISTICS

The specifications are $T_a = 25^{\circ}\text{C}$.

$V_{in} = 19\text{V} / 12\text{V}$, $V_{out} = 1.5\text{V}$, $R_{TONI} = 1\text{ M Ohms}$ (integrated)

$C_{in} = 150\mu\text{F}/25\text{V}\times 1$, $10\mu\text{F}/25\text{V}\times 1$, $0.1\mu\text{F}/25\text{V}\times 1$, $C_{out} = 330\mu\text{F}/6.3\text{V}$ (ESR=10m Ohms) $\times 1$, $10\mu\text{F}/25\text{V}\times 3$

Input Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{Q(VIN)}$	Input supply bias current	$I_{out} = 0\text{A}$ $V_{out} = 1.5\text{V}$, $V_{in} = 19\text{V}$, EN/PSV = 5V $V_{in} = 19\text{V}$, EN/PSV = Tri-stated $V_{in} = 12\text{V}$, EN/PSV = 5V $V_{in} = 12\text{V}$, EN/PSV = Tri-stated	-	0.1 20 0.1 25	-	mA
$I_{S(VIN)}$	Input supply current	$I_{out} = 7\text{A}$, $V_{out} = 1.5\text{V}$, $V_{in} = 19\text{V}$ $V_{in} = 12\text{V}$	-	0.69 1.06	-	A
Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range	$V_{in} = 19\text{V}$, $V_{out} = 1.5\text{V}$	0	-	7	A
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	EN/PSV = Tri-stated, $V_{in} = 1.8\text{V}$ to 25V $V_{out} = 1.5\text{V}$, $I_{out} = 0\text{A}$ $V_{out} = 1.5\text{V}$, $I_{out} = 7\text{A}$	-	0.1 0.1	-	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation accuracy	EN/PSV = Tri-stated $I_{out} = 0\text{A}$ to 7A $V_{out} = 1.5\text{V}$ $V_{in} = 19\text{V}$, $V_{in} = 12\text{V}$,	-	1	-	%
$V_{OUT(AC)}$	Output ripple voltage	EN/PSV = Tri-stated, $I_{out} = 7\text{A}$ $V_{out} = 1.5\text{V}$, $V_{in} = 19\text{V}$, $V_{in} = 12\text{V}$	-	60	-	mVp-p
Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	$I_{out} = 10\%$ to 90% of 7A. Current slew rate = 2.5A/uS $V_{in} = 19\text{V}$, $V_{out} = 1.5\text{V}$ $V_{in} = 12\text{V}$, $V_{out} = 1.5\text{V}$	-	100	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	$I_{out} = 90\%$ to 10% of 7A. Current slew rate = 2.5A/uS $V_{in} = 19\text{V}$, $V_{out} = 1.5\text{V}$ $V_{in} = 12\text{V}$, $V_{out} = 1.5\text{V}$	-	100	-	mVp-p

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Control Stage						
PVCC	Supply voltage		4.5	5.0	5.5	V
I _{PVCC}	PVCC operating current	EN/PSV = Tri-stated I _o = 7A	-	15	-	mA
V _{FBTHR}	FB turn-on threshold voltage	PVCC = 4.5V to 5.5V	0.494	0.5	0.506	V
R _{TONI}	Internal resistor between Vin and TON pins		0.99	1	1.01	MΩ
TON	PWM on-time	V _{in} = 19V, V _{out} = 1.5V, I _{out} = 7A R _{TONI} = 1 MΩ (intergated)	-	300	-	nS
V _o	Output voltage range		-	0.5	PVCC	V
R _{FBHI}	Internal resistor between Vout and FB pins		9.9	10	10.1	kΩ
V _{ENL}	EN low threshold voltage	EN/PSV low	-	1.2	-	V
V _{ENT}	EN tri-stated voltage	EN high, PSV low	-	2	-	V
V _{ENH}	EN high threshold voltage	EN/PSV high	-	3.1	-	V
Fault Protection						
R _{SENI}	Internal resistor between ISEN and PHASE pins		17.91	18	18.09	kΩ
V _{UVF}	Output under voltage fault		-20	-10	-5	%
V _{OVF}	Output over voltage fault		+15	+20	+40	%
PVCC _{UVTHR}	PVCC under voltage threshold	Falling (100mV Hysteresis)	3.7	4.0	4.3	V
TP _{OTPL}	Over temperature lockout		-	165	-	°C
PGOOD Stage						
V _{PGDLV}	PGOOD low output voltage	Sink 1mA	-	-	0.4	V
V _{PGDUVTHR}	PGOOD under voltage threshold		-12	-10	-8	%

TYPICAL PERFORMANCE CHARACTERISTICS

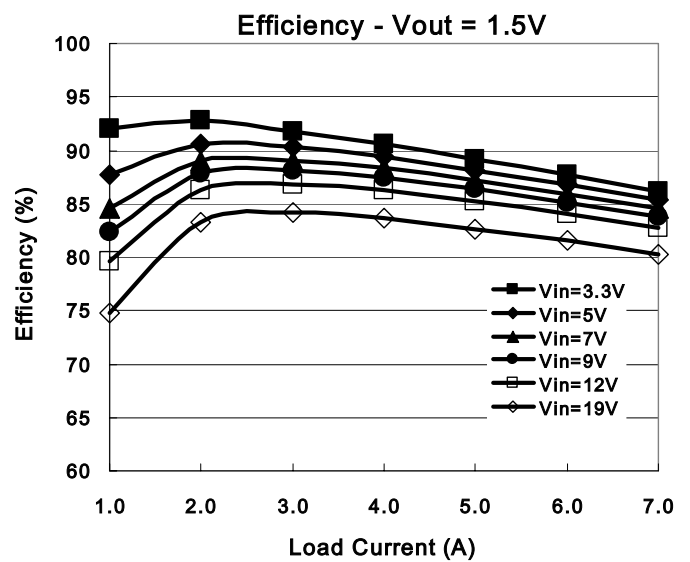
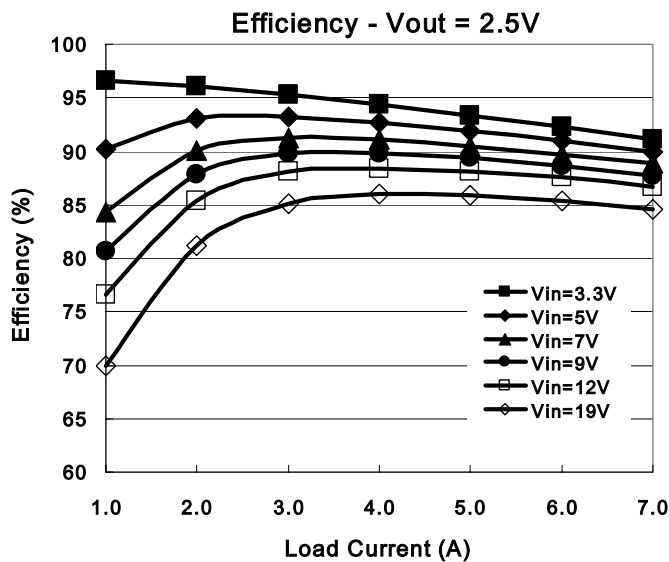
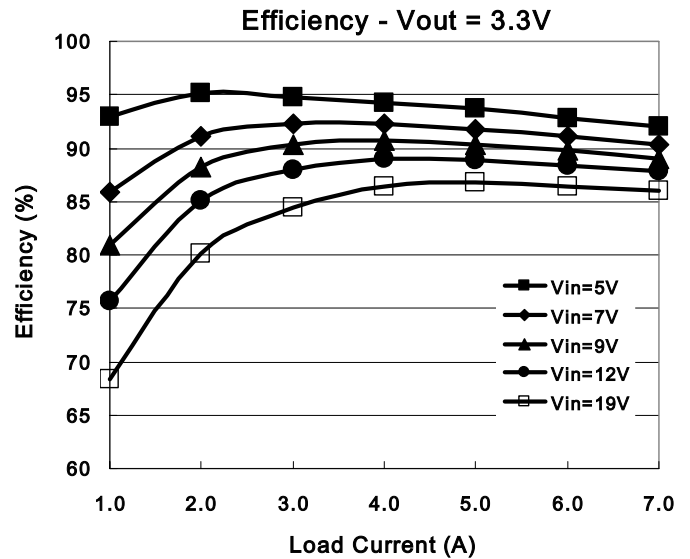
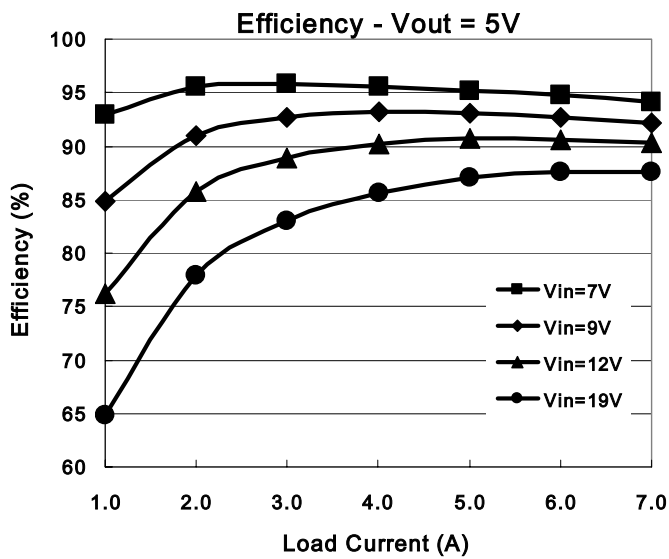
Efficiency Performance:

Test Condition : $T_a = 25^\circ\text{C}$.

Demo board size : 114.5mm×101.5mm×1.6mm, 4layers

$R_{\text{TONI}} = 1 \text{ M Ohms}$ (integrated), EN/PSV = Tri-stated

$C_{\text{in}} = 150\mu\text{F}/25\text{V}\times 1, 10\mu\text{F}/25\text{V}\times 1, 0.1\mu\text{F}/25\text{V}\times 1, C_{\text{out}} = 330\mu\text{F}/6.3\text{V}$ (ESR=10m Ohms) $\times 1, 10\mu\text{F}/25\text{V}\times 3$



TYPICAL PERFORMANCE CHARACTERISTICS

Power Saving Mode:

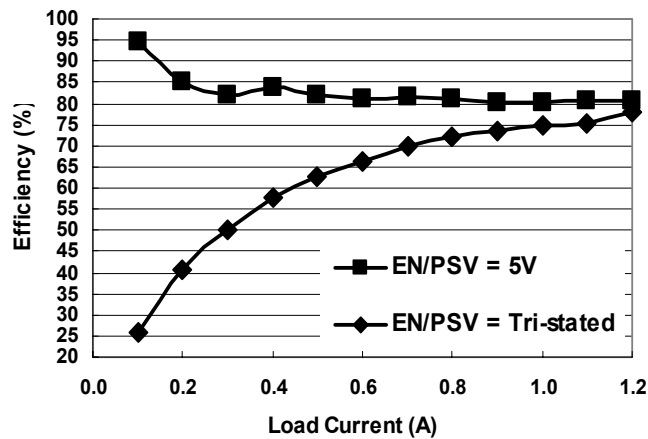
Test Condition : $T_a = 25^\circ\text{C}$

Demo board size : 114.5mm×101.5mm×1.6mm, 4 layers

$V_{in} = 19\text{V}$, $V_{out} = 1.5\text{V}$, $R_{TONI} = 1\text{ M Ohms}$ (integrated)

$C_{in} = 150\mu\text{F}/25\text{V}\times 1$, $10\mu\text{F}/25\text{V}\times 1$, $0.1\mu\text{F}/25\text{V}\times 1$, $C_{out} = 330\mu\text{F}/6.3\text{V}$ (ESR=10m Ohms) $\times 1$, $10\mu\text{F}/25\text{V}\times 3$

Efficiency with EN/PSV Different Setting



Transient Response Performance:

Test Condition : $T_a = 25^\circ\text{C}$

Demo board size : 114.5mm×101.5mm×.6mm, 4 layers.

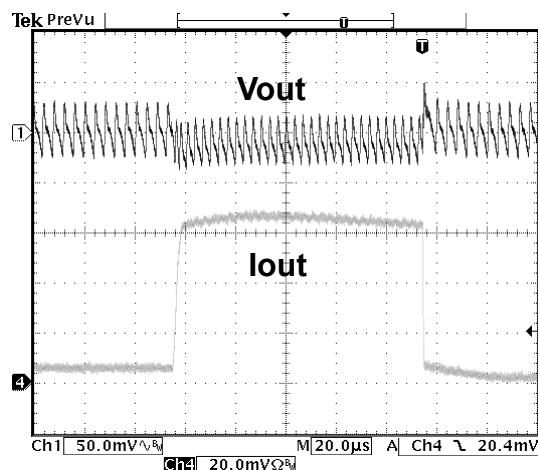
$V_{in} = 19\text{V}$, $V_{out} = 1.5\text{V}$, $R_{TONI} = 1\text{ M Ohms}$ (integrated), EN/PSV = Tri-stated

$C_{in} = 150\mu\text{F}/25\text{V}\times 1$, $10\mu\text{F}/25\text{V}\times 1$, $0.1\mu\text{F}/25\text{V}\times 1$,

$C_{out} = 330\mu\text{F}/6.3\text{V}$ (ESR = 10m Ohms) $\times 1$, $10\mu\text{F}/25\text{V}\times 3$, $1\mu\text{F}\times 1$, $0.1\mu\text{F}\times 1$

$I_{out} = 10\%$ to 90% and 90% to 10% of full load (7A).

Current slew rate = 2.5A/uS



PIN FUNCTIONS

AGND Pin- 1, 2, 3, 4

Signal common of the HM07105. The signals are referred to the AGND pin. All of small-signal components can connect to the ground plane immediately; it does not need more long distance or resistor connects to power ground.

PVCC Pin- 5, 6

The PVCC pin is the supply voltage input. There is no LDO to supply PWM controller and gate driver inside the module. Therefore, HM07105 requires additional +5V bias voltage to offer all of functions. This +5V bias supply can be generated by linear regulator. In order to make this +5 bias voltage stable, it needs a 2.2 μ F MLCC (C_{PVCC}) bypass capacitor respect to PVCC pin to the AGND pin. The user can refer to Figure 2 typical application schematic and application note.

ISEN Pin- 7

The ISEN pin is the input for the over current protection (OCP) setting. Which compares $R_{DS(ON)}$ of low-side MOSFET to set over current threshold. The HM07105 has initial protect over current limit. It is integrated internal 18k Ohms resistance (R_{SENI}) between ISEN and PHASE pins which can avoid significant over current impact to module. Besides, it also can connect additional resistor R_{SEN} between the ISEN pin and the PHASE pin that changes the current limit point by paralleling. Select the value of R_{SEN} that will force the ISEN pin to source the ISEN

threshold current when the inductor current reaches the desired OCP set point.

TON Pin- 8

The TON pin programs the PWM switching frequency and delivers input voltage signal to constant on-time one shot logic controller. It determined the high-side switch turn-on time. The HM07105 has initial set this parameter to approach integrated completely. It is included internal 1M Ohms resistance (R_{TONI}) between VIN and TON pins which can provide initial switching frequency and on-time for module. Besides, it also can connect additional resistor R_{TON} between VIN and TON pins that change the switching frequency and on-time by paralleling.

VIN Pin- 9

Power input pin. Apply input voltage between VIN pin and PGND pin. Recommend placing input decoupling capacitance directly between VIN pin and PGND pin. Besides, the input capacitor should locate to module as closely as possible.

PHASE Pin- 10

The PHASE pin is the switching node between high and low side MOSFET. It also returns the current path for the high side MOSFET driver. And detecting the low-side MOSFET drain voltage for the over current limits point.

PIN FUNCTIONS

PGND Pin- 11

Power ground pin for both input and output return path. It needs to connect one (or more) ground plan immediately which is recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation.

VOUT Pin- 12

Power Output Pin. Apply output load between this pin and PGND pin. Recommend placing high frequency output decoupling capacitance directly between this pin and PGND pin. Besides, the output capacitor should locate to module as closely as possible.

EN / PSV Pin-13

The EN/PSV pin is enables the supply. It also can select the power saving mode or not depends on its voltage level. When EN/PSV is tied to PVCC, the HM07105 is enabled and power saving mode will be enabled. When the EN/PSV pin is open, an internal pull-up will activate the HM07105 and power saving mode will be disabled.

FB Pin- 14

The FB pin is output voltage adjustment of the HM07105. It will regulate to 0.5V at the FB pin respect to the AGND pin. The HM07105 has integrated voltage dividing resistor of top side. This is precision 10k Ohms resistance (R_{FB1}) between VOUT and FB pins. Different output voltage can be programmed with additional resistor between FB to AGND. On the other hand, the capacitor of between FB and VOUT

pins controls output ripple content at feedback pin. It will affect the stability of power converter. Therefore, the R_{FB} resistor and C_{FB} capacitor should locate to module as closely as possible. The user can refer to Figure 2 typical application schematic and application note.

PGOOD Pin- 15

The PGOOD pin is an open-drain output and requires a pull-up resistor. When the output voltage is 20% above or 10% below its set voltage, PGOOD pin gets polled low. It is held low until the output voltage returns to within these tolerances once more.

REFERENCE CIRCUITRY FOR GENERAL APPLICATION

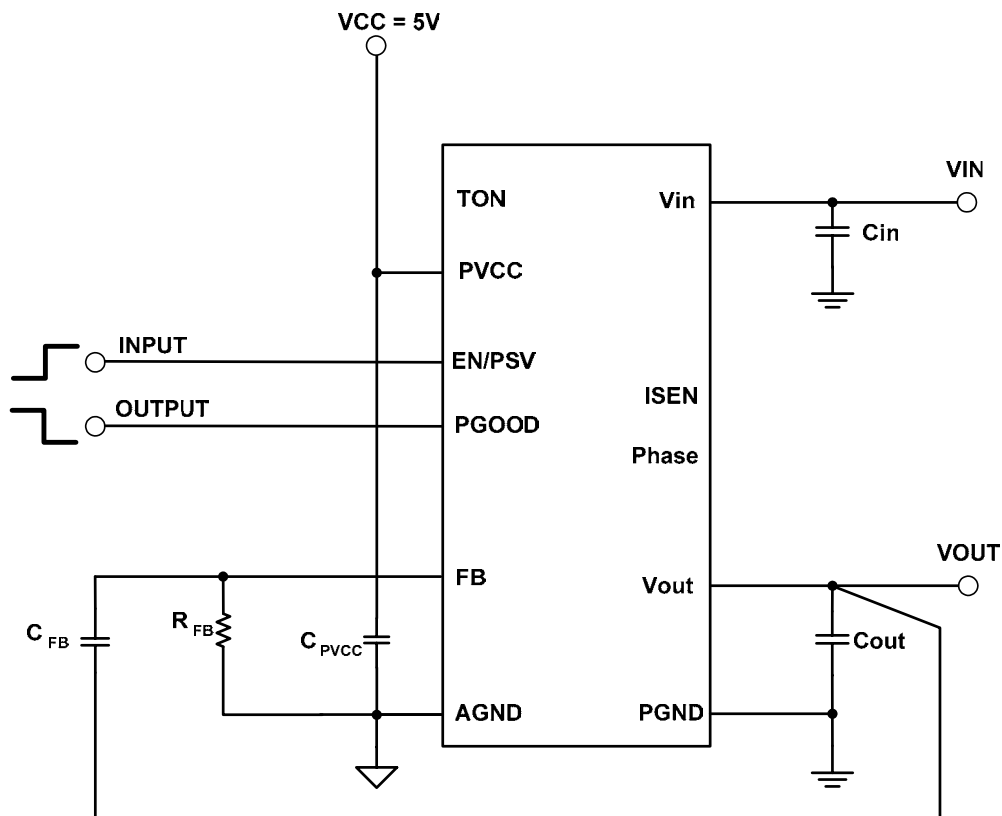


Figure 2. Typical Application Schematic

APPLICATION INFORMATION

The typical HM07105 application circuit is shown in Figure 2. External component selection is primarily determined by the maximum load current and input / output voltage.

Programming the Output Voltage

The HM07105 has an internal $0.5V \pm 1.2\%$ reference voltage. It only programs the dividing resistance R_{FB} which respects to FB pin and AGND. The output voltage can be regulated as

$$V_{out} = 0.5 \times \left(1 + \frac{10k}{R_{FB}} \right)$$

Note : HM07105 has integrated 10k Ohms resistance into module.(Dividing resistor for top side). The resistance respects to different output voltage are as following.

Vout	0.9V	1.05V	1.2V	1.5V
R _{FB}	12.5k	9.09k	7.143k	5k

Vout	1.8V	2.5V	3.3V	5V
R _{FB}	3.84k	2.5k	1.786k	1.11k

Programming the Pseudo-Fixed PWM Switching Frequency with Constant On-time Control

The PWM control architecture consists of a constant on-time, pseudo-fixed frequency controller. The output voltage ripple developed across the output capacitor's ESR provides the PWM ramp signal eliminating. The high-side switch on-time is determined by one-shot whose period is directly proportional to output voltage and inversely proportional to

input voltage. A second one shot sets the minimum off-time which is typically 400nS. The on-time one shot comparator has two inputs. One input looks at the output voltage (V_o), while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for voltage on this capacitor to charge from zero to output voltage (V_o), thereby making the on-time of the high-side switch. This implementation results in a nearly constant switching frequency without need for a clock generator.

Duty cycle will be decided by below formula:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T}$$

Where :

D is the duty cycle.

V_{OUT} is the output voltage.

V_{IN} is the input voltage.

T_{ON} is the high-side switch on-time.

T_{OFF} is the high-side switch off-time.

T is period of PWM.

When the PWM switching frequency is determined, thereby the PWM period is inversely proportional to switching frequency as below. Then, high-side switch on-time (T_{ON}) can be calculated by duty and period of PWM.

$$T = \frac{1}{F_s}$$

$$T_{ON} = \frac{V_{OUT}}{F_s \times V_{IN}}$$

Where :

F_s is the switching frequency.

APPLICATION INFORMATION

Based on high-side switch on-time (T_{ON}), the PWM switching frequency decides on a resistor (R_{TON}) which connects from input voltage (V_{IN}) to the TON pin. In accordance with different output voltage the formula for

$0.5V < V_{OUT} < 3.3 V$:

$$T_{ON} = 3.3 \times 10^{-12} \times (R_{TON} + 37 \times 10^3) \times \left(\frac{V_{OUT}}{V_{IN}} \right) + 50nS$$

$3.3V < V_{OUT} < 5 V$:

$$T_{ON} = 0.85 \times 3.3 \times 10^{-12} \times (R_{TON} + 37 \times 10^3) \times \left(\frac{V_{OUT}}{V_{IN}} \right) + 50nS$$

Where :

R_{TON} is equivalent resistance between V_{in} and TON pins.

Note: HM07105 has integrated 1M Ohms resistance (R_{TONI}). Due to the HM07105 has internal set 1M Ohms inside the module. Therefore, the equivalent resistance of R_{TON} is

$$R_{TON} = \left(\frac{\text{External } R_{TON} \times R_{TONI}}{\text{External } R_{TON} + R_{TONI}} \right)$$

+5V Bias Supplies Connection

The HM07105 requires an external +5V bias supply in addition to system power. It supplies PWM controller and high / low side MOSFET gate driver. The +5V bias supply can be generated with an external linear or regulator or power supply devily. It needs at least 2.2uF MLCC decoupling capacitor close to PVCC pin with respects to AGND.

Enable and Power Saving Mode (EN/PSV)

The EN/PSV pin enables the HM07105. When the EN/PSV is tied to PVCC, the module is enabled and power saving mode also be enabled. When the EN/PSV pin is tri-stated, this state will activate the module and power save will be disabled. If power saving mode is enabled, the power saving comparator will look for inductor current to cross zero whether is on eight consecutive switching cycles by comparing the phase node (Phase) to PGND. Once observed, the module will enter power saving mode and turn off low-side MOSFET when the current crosses zero. To improve light-load efficiency and add hysteresis, the on-time is increased by 50% in power saving mode for pulse skip. The efficiency improvement as light-loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the module will immediately exit power saving mode. The HM07105 can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps even when power saving mode is enabled.

Soft Discharge

The HM07105 has soft discharge function for output energy when EN/PSV pin is pulled low (disable). This will ensure that the output is in a defined state next time; it is enabled and also ensures that there are on dangerous negative voltage excursions to be concerned about.

APPLICATION INFORMATION

Power GOOD Output

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 20% above 10% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. PGOOD is also held low during start-up and will not be allowed to transient high until soft start is over (440 switching cycles) and the output reaches 90% of its set voltage. There is a 5uS delay built into the PGOOD circuitry to prevent false transitions.

Output Over-Voltage Protection

When the output exceeds 20% of its set voltage then the low-side MOSFET is latched on. That is discharging output energy to low side MOSFET which is in order to avoiding high voltage to damage the load. It stays latched on and the module is latched off until reset. There is a 5uS delay built into the over voltage protection circuit to prevent false transitions.

Output Under-Voltage Protection

When the output voltage is 10% below its set voltage the output is latched in tri-stated condition. It stays latched and the module is latched off until reset. There is a 5uS delay built into the under voltage protection circuit to prevent false transitions.

Note 3 : To reset from any fault, PVCC or EN/PSV must be toggled.

Over-Temperature

When an OTP fault is detected, the HM07105 over temperature protection circuit suspends PWM, but will not affect the PGOOD pin, or latch off the HM07105. The over temperature protection circuit measures the temperature of the silicon and activates when the rising threshold temperature TP_{OTPL} has been exceeded.

Power-On Reset, UV Lockout and Soft Start

An internal power-on reset (POR) occurs when PVCC exceeds 3V, starting up the internal biasing. PVCC under voltage lockout (UVLO) circuitry inhibits the module until PVCC rises above 4.2V. At this time the UVLO circuitry resets the fault latch and soft-start counter, and allows switching to occur if the device is enabled. Switching always starts with low-side switch signal to charge up the bootstrap capacitor. With the soft-start circuit (automatically) it will progressively limit the output current (by limiting the current out of the ISEN pin) over a predetermined time period of 440 switching cycles.

The ramp occurs in four steps:

- (1) 110 cycles at 25% ISEN with double minimum off-time (for purposes of the on-time one-shot, there is an internal positive offset of 120mV to VOUT during this period to aid in startup).
- (2) 110 cycles at 50% ISEN with normal minimum off time.
- (3) 110 cycles at 75% ISEN with normal minimum off-time.
- (4) 110 cycles at 100% ISEN with normal minimum off time.

APPLICATION INFORMATION

At this point the output under-voltage and power good circuitry is enabled. There is 100mV of hysteresis built into the UVLO circuit and when PVCC falls to 4.1V (nom.) the output drivers are shut down and tri-stated.

Current Limit

Current limiting of the HM07105 can be accomplished by sensing voltage for on-state resistance of low-side MOSFET. $R_{DS(ON)}$ sensing is more efficient and less expensive. R_{SEN} resistor between the ISEN pin and PHASE pin sets the over current threshold. This resistor R_{SEN} is connected to a $10\ \mu\text{A}$ current source within the module which is turned on when the low side MOSFET turns on. When the voltage drop across the low side MOSFET equals the voltage across the R_{SEN} resistor, positive current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the low-side MOSFET falls below the voltage across the R_{SEN} resistor. In an extreme over-current situation, the top MOSFET will never turn back on and eventually the part will latch off due to output under-voltage (see Output Under-voltage Protection). The current sensing circuit actually regulates the inductor valley current (see Figure 3). This means that if the current limit is set to 7A, the peak current through the inductor would be 7A plus the peak ripple current, and the average current through the inductor would be 7A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are

shown as below:

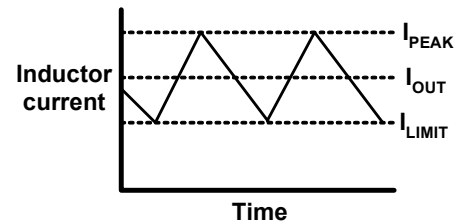


Figure 3. Valley current limiting

The equation for the current limit threshold is

$$I_{SEN} = 10 \times 10^{-6} \times \left(\frac{R_{SEN}}{R_{DS(ON)}} \right) \text{A}$$

The current limit looks at the “valley current” (I_{VALLEY}), which is average output current minus half the ripple current. The valley current is

$$I_{VALLEY} = I_{OUT} - \left(\frac{I_{RIPPLE}}{2} \right) \text{A}$$

Where : I_{RIPPLE} is $I_{PEAK} - I_{LIMIT}$.

Therefore, the current limit resistor (R_{SEN}) can be calculated by output current and valley current as

$$R_{SEN} = 1.4 \times I_{VALLEY} \times \left(\frac{R_{DS(ON)}}{10 \times 10^{-6}} \right) \text{Ohms}$$

Where :

R_{SEN} is equivalent resistance between PHASE and ISEN pins.

$R_{DS(ON)}$ is typically 10m ohm ($V_{GS}=4.5V$, $I_{DS}=30A$).

Note: HM07105 has integrated 18k Ohms resistance (R_{SENI}). Therefore, the equivalent resistance of R_{SEN} is

$$R_{SEN} = \left(\frac{\text{External } R_{SEN} \times R_{SENI}}{\text{External } R_{SEN} + R_{SENI}} \right)$$

APPLICATION INFORMATION

The current limit circuitry also protects against negative over-current (i.e. when the current is flowing from the load to PGND through the inductor and low-side MOSFET). In this case, when the low-side MOSFET is turned on, the phase node, (Phase), will be higher than PGND initially. The HM07105 monitors the voltage at Phase, and if it is greater than a set threshold voltage of 125mV (nom.) the low-side MOSFET is turned off. The device then waits for approximately 2.5 μ s and then LG goes high for 300ns (typ.), once more to sense the current. This repeats until either the over current condition goes away or the part latches off due to output over-voltage (see Output Over-voltage Protection).

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power up. The HM07105 provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by the following formula :

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V}$$

Where :

C_{IN} is the input capacitance (μ F)

I_{IN} is the input current (A)

Δt is the turn on time of the high-side switch (μ s)

ΔV is the allowable peak to peak voltage (V)

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain terminal of the high side MOSFET and the source terminal of the low side MOSFET, in order to reduce the voltage ringing created by the switching current across parasitic circuit elements.

Output Capacitors

The HM07105 is designed for low output voltage ripple. The bulk output capacitors C_{OUT} is chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical capacitance is 330 μ F, if all ceramic output capacitors are used. The internally optimized loop compensation provides sufficient stability margin for all ceramic capacitors applications. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required.

APPLICATION INFORMATION

Timing Chart

The timing chart can be helpful for engineers to see the operation of each pin of HM07105 and can be used to be the primary basis during the error detection. The timing chart of HM07105 during the normal operation is as follows:

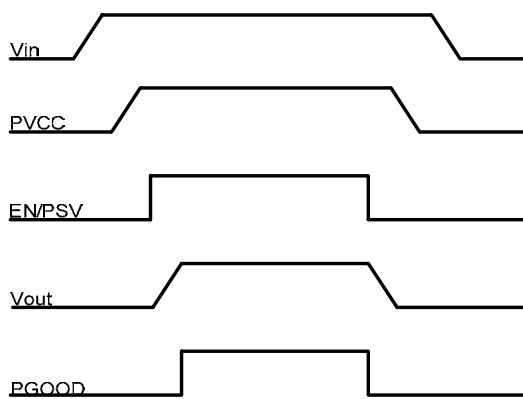


Figure 4. Normal Operation

When it comes to start-up, it should be noted that the internal mechanism of HM07105 does not allow the startup of PVCC to be faster than that of the input voltage, so in order to make it work normally, this problem should be avoided in applications.

Furthermore, when the protection of HM07105 occurs, its timing chart can be further categorized into three types. One is that when the output over voltage occurs, the PGOOD terminal will convert from the high level to the low level and output will be turned off if the output voltage is higher than the protection point. If the fault condition is clear, the output can be re-starting by EN pin. The timing for each pin is as follows:

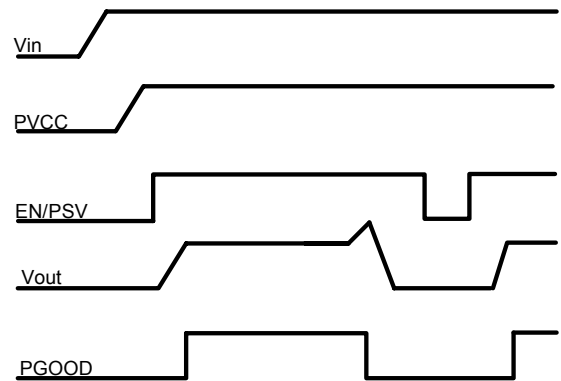


Figure 5. Output Over Voltage

APPLICATION INFORMATION

Another is that when the output under voltage, output over current and output short circuit occur, the output voltage will drop down. When the output voltage descends to the protection point, PGOOD will convert from the high level to the low level. If the fault condition is clear, the output can be re-starting by EN pin. Its timing chart is as follows:

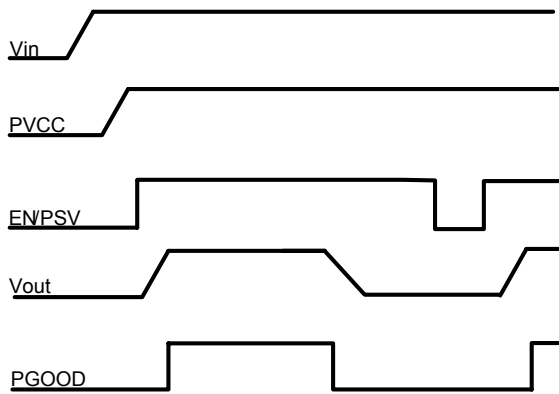


Figure 6. Output Under Voltage, Output Over Current, and Output Short Circuit

The other is that when the input under voltage occurs, output voltage will start to drop down if the input voltage descends to the protection point. When the decline of the output voltage exceeds the allowed range, PGOOD will convert from the high level to the low level. If the fault condition is clear, the output can be re-starting by EN pin. Its timing chart is as follows:

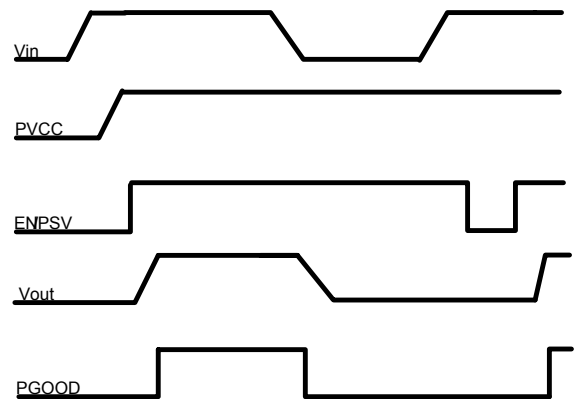


Figure 7. Input Under Voltage

APPLICATION INFORMATION

MOSFET Stress Consideration

The HM series module has ultra small switching loop in input and output circuit than discrete components solution. It can reduce the stray effects as leakage inductor and capacitor in the switching loop. Resulting resonance voltage overshoot across the MOSFETs can be reduced effectively.

Even through the resonant voltage overshoot can be controlled, but it is still possible beyond the voltage rating of MOSFETs due to different PCB layout and input/output voltage condition. Therefore, sunbber circuit can be implemented between PHASE and PGND pins of module to clamp the voltage overshoot to increase the reliability of module.

For example as Figure 8 shows the waveform of voltage spike across MOSFET. Figure 9 shows the waveform of voltage spike across MOSFET improved by snubber circuit.

The design shows on Figure 10 is just an example for reference. The designer still need to adjust the circuitry to trade off the efficiency and design margin according to the actual condition.

Voltage spike over V_{DS} of MOSFET

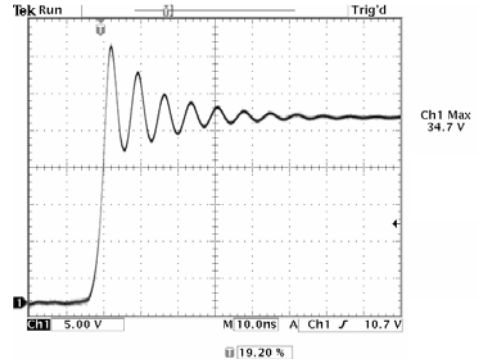


Figure 8 MOSFET V_{DS} Waveform Without Snubber Circuit

Voltage spike below V_{DS} of MOSFET after improved.

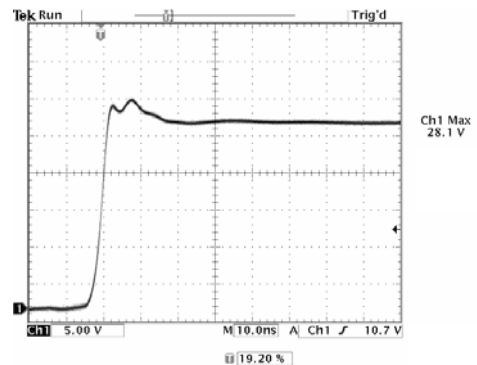


Figure 9 MOSFET V_{DS} Waveform With Snubber Circuit

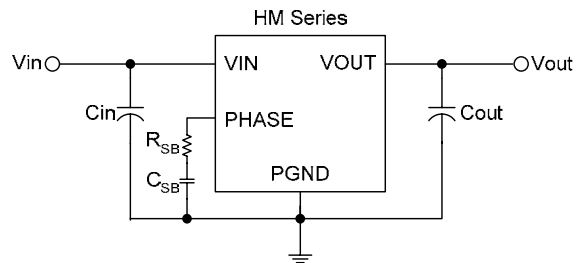


Figure 10 Schematic of Snubber Circuit ($R_{SB} = 2.2\Omega$, $C_{SB} = 4700\text{pF}$)

APPLICATION INFORMATION

Thermal Consideration and Output Current De-rating

All of thermal testing condition is complied with JEDEC EIA/JESD 51 Standards. Therefore, the test board size is 114.5mm*101.5mm*1.6mm with 4 layers. The case temperature of module sensing point is shown as Figure 11. Then $R_{th(j-a)}$ and $R_{th(j-c)}$ are measured with the component mounted on a effective thermal conductivity test board on 0 LFM condition.

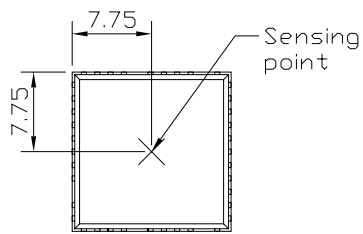


Figure 11. Case temperature sensing point
(Top view)

The HM07105 module is packaged in 15x15x3.5mm QFN package that are constructed with copper lead frames that have exposed thermal pads. The output ability is function of input voltage/current, output voltage/current and ambient temperature factor etc. For long-term reliability, HM07105 module is designed for using when the case temperature is below 110°C for long term operating consideration. Although the limitation of junction temperature of semiconductor devices is up to 150°C. In Figure 12 and Figure 13, the power loss curves can be used in coordination with each load current.

The Figure 14 and 15 are 1.5V output voltage de-rating curves respectively for 12V and 19 V input. The Figure 16 and 17 are 3.3V output voltage de-rating curves respectively for 12V and 19 V input. In Figure 12 and 13, the power loss curves can be used in coordination with each load current. It would be convenient for user to confirm and estimate modular's approximate performance according to actual operating conditions in beginning of design.

APPLICATION INFORMATION

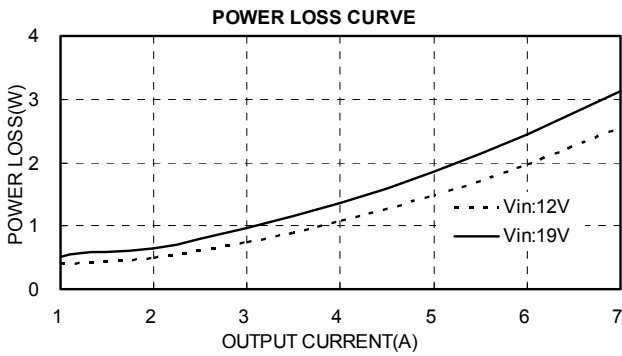


Figure 12. 1.5Vo Power Loss Curves

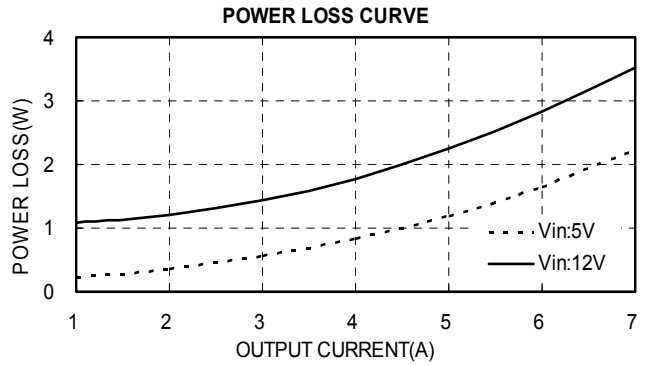


Figure 13. 3.3Vo Power Loss Curves

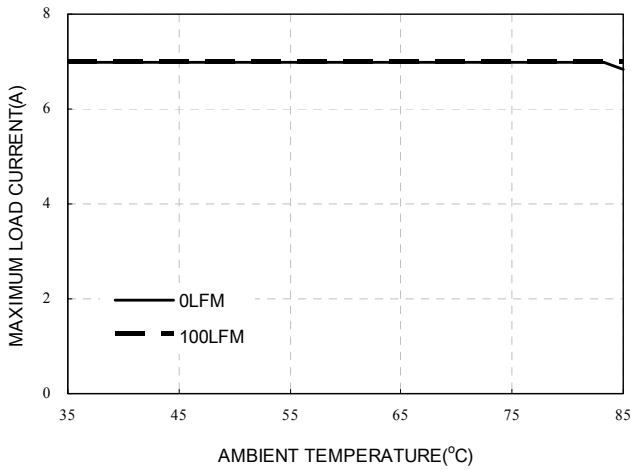


Figure 14. 12Vin, 1.5Vout De-rating Curves

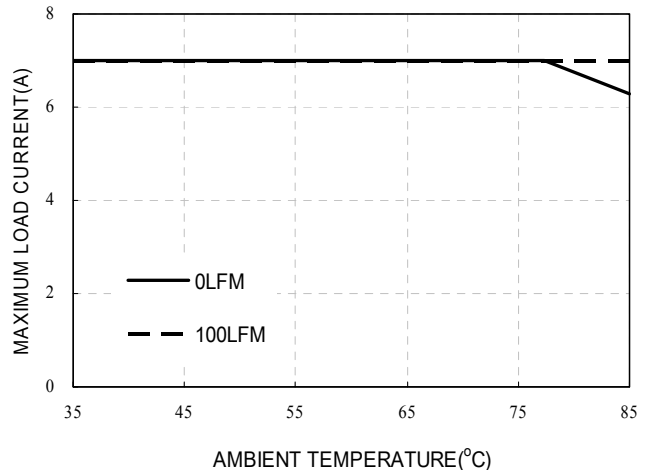


Figure 15. 19Vin, 1.5Vout De-rating Curves

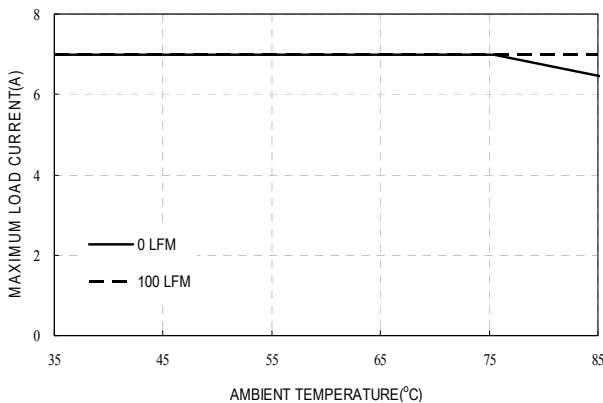


Figure 16. 12Vin, 3.3Vout De-rating Curves

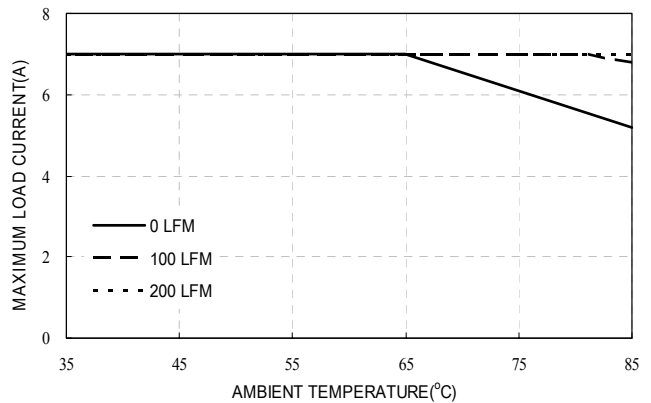
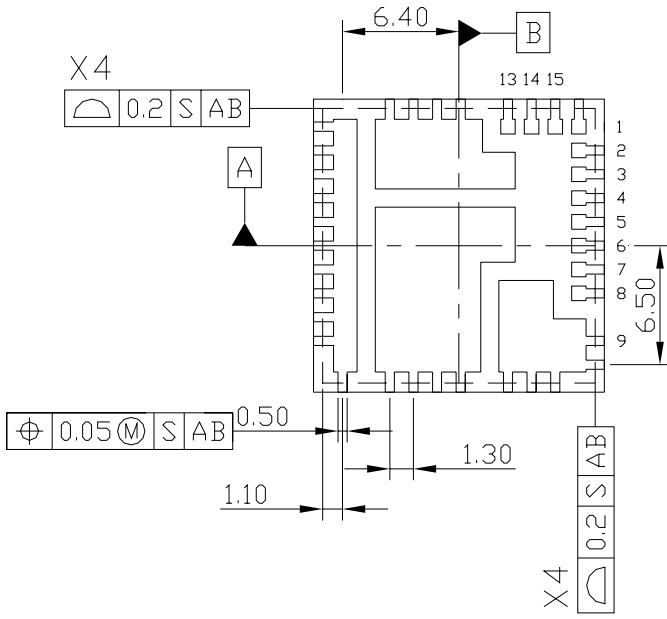


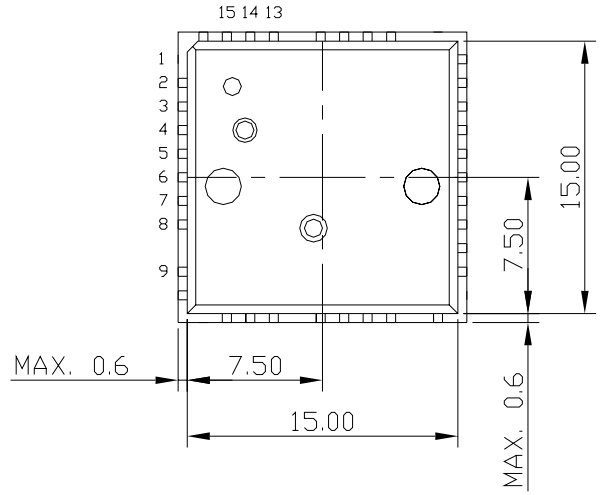
Figure 17. 19Vin, 3.3Vout De-rating Curves

PACKAGE DIMENSION

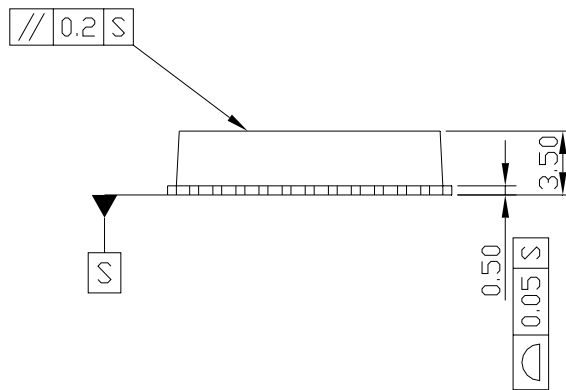
Unit:mm



Bottom View



Top View

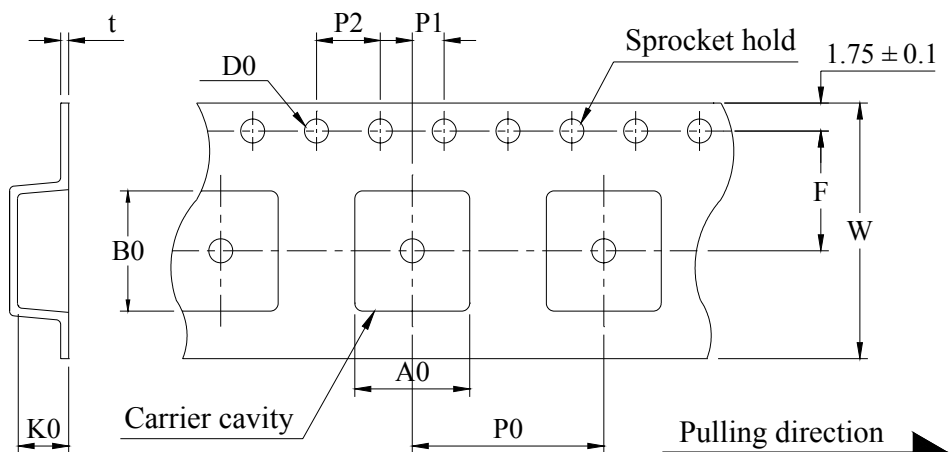


Side View

QFN PACKING INFORMATION

Tape Packaging Dimensions

Unit:mm



For QFN 15x15

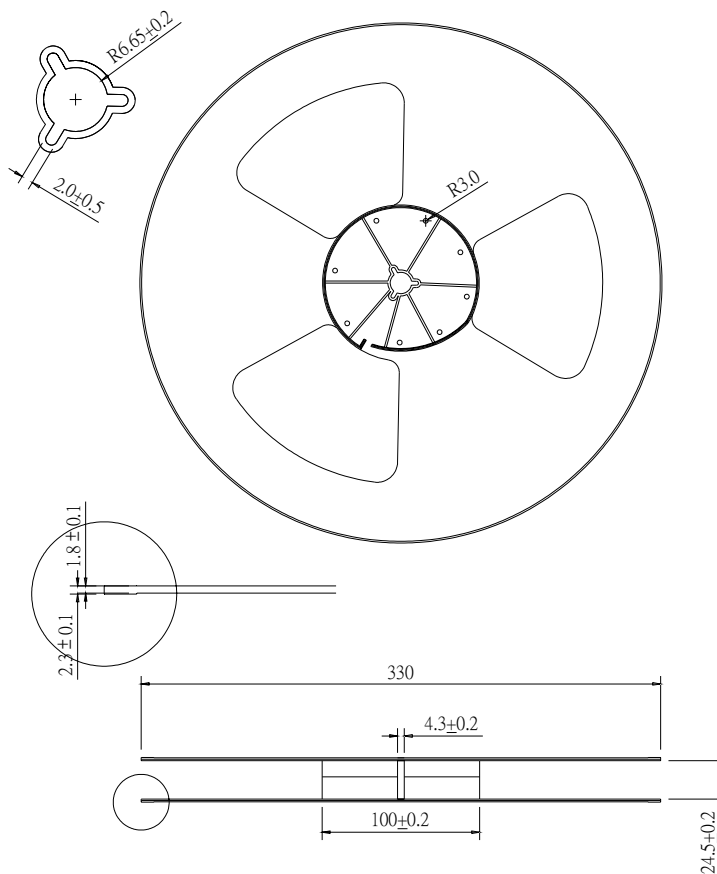
Unit:mm

A0	16.20 ± 0.10	t	0.30 ± 0.05
B0	16.20 ± 0.10	K0	3.70 ± 0.10
F	11.5 ± 0.10	P0	20.00 ± 0.10
W	24.00 ± 0.30	P1	2.00 ± 0.10
D0	φ1.55 ± 0.05	P2	4.00 ± 0.10

QFN PACKING INFORMATION

Reel Dimensions

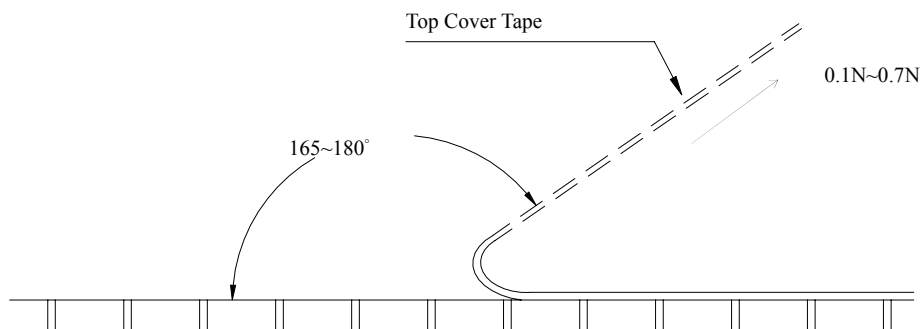
Unit:mm



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1 to 0.7N



QFN Packing Information

Number of Taping

500 pieces / reel

Label Marking

The following items shall be marked on the reel.

- a. Type designation
- b. Quantity
- c. Parts / No.
- d. Lot / No.

The following items shall be marked on the static shielding bag

- a. Caution Marking
 - 1. Level class : 3
 - 2. Peak body temperature
 - 3. Bake requirement

b. MSID Marking

- 1. Moisture sensitive Logo

c. Seal Label

- 1. Seal date

d. Production Label

- 1. Type designation
- 2. Quantity
- 3. Parts / No.
- 4. Lot / No.

e. Shipping Label

- 1. *Customer's name
- 2. *Customer's part No.
- 3. Manufacturer's part No.
- 4. Manufacturer's name
- 5. Manufacturer's country

*Note 4 : Item (1) and (2) listed by request

PACKAGE DESCRIPTION

Introduction

The structure of HM07105 belongs to Quad-Flat pack-No leads package (QFN). This kind of package has some advantages like good thermal and electrical conductivity, low weight, small size, etc. As QFN structure is suitable for surface mounting technology, more and more uses in industry are concerned recently.

This reference shows the PCB layout pattern design, stencil pattern design and reflow profile parameters. It is noted that these guidelines are general design rules. Users could modify parameters according to their real application.

HM07105 contains several types of devices. There are resistor, capacitor, inductor and control IC. The bottom of HM07105 is lead-frame footprint that transmits electrons and heat effectively. And polymer compound is covered and formed on the module to protect these devices. The module has a small size of 15x15x3.5 mm.

(Figure 18, Figure 19, Figure 20)

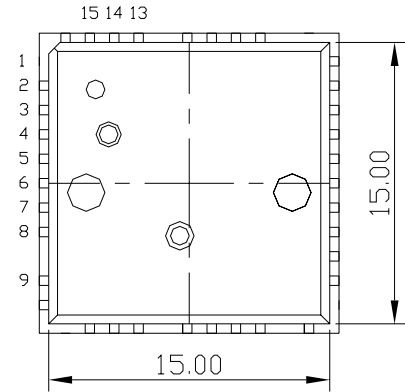


Figure 18. Top View

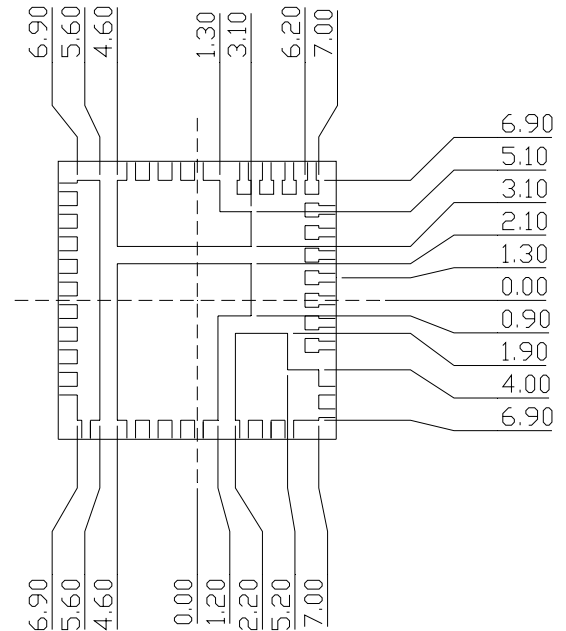


Figure 19. Bottom View

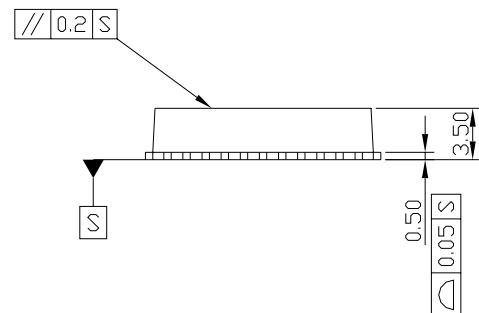


Figure 20. Side View

PACKAGE DESCRIPTION

PCB Layout Pattern Design

The bottom of HM07105 is lead-frame footprint, which could be attached to PCB by surface mounting process. Figure 21 shows the PCB layout pattern. The PCB layout pattern has an extended distance of 1.3mm toward outside. But the distance between PCB pads is still kept in 1mm, the same as lead-frame design. This idea is to help soldering more completely. It is suggested that user designs smaller PCB layout pattern with corresponding HM07105 to avoid forming short circuit when soldering. However, the reduction percentage of each pad area of the PCB layout pattern is not equal. Large pads of the pattern are usually reduced more area and small pads have less reduction.

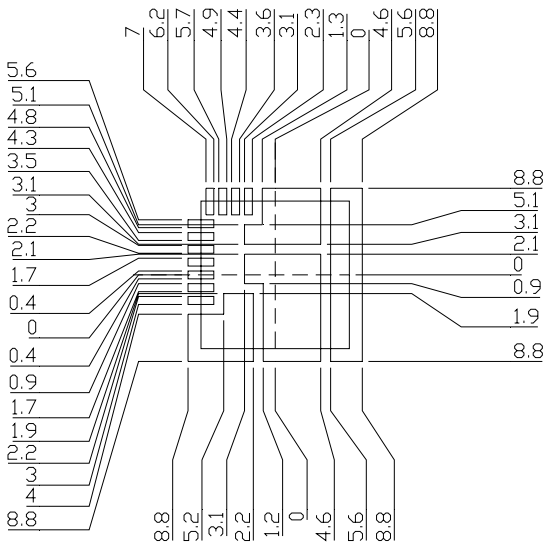


Figure 21. Recommended PCB Layout Pattern

Stencil Pattern Design

Solder-printing method is very popular in surface mounting process. The stencil pattern design affects soldering very much. Figure 22 and Figure 23 are two examples of stencil pattern, which Figure 22 uses circle pads and Figure 23 uses square pads.

No matter circle or square pads, they have similar design rules. The gap width between pad to pad is 0.6mm. User should consider the symmetry of the whole stencil pattern when designing its pads. Designing larger pads for the stencil pattern would be a better choice. It is recommended that the stencil printing area should be 55% to 75% coverage of the total PCB layout pattern. 0.1mm thickness of stencil is also recommended for the use of printing so that the solder thickness could reach about 120 μ m, a proper solder thickness.

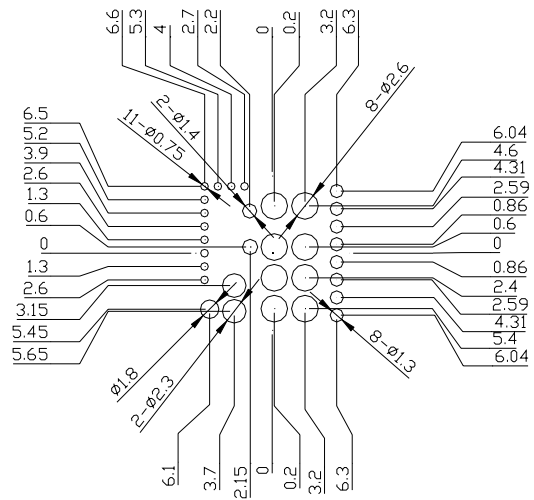


Figure 22. Stencil Pattern with Circle Pads

PACKAGE DESCRIPTION

Reflow Parameters

Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. Figure 24 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C the ramp rate of temperature should be not more than 1.5°C/sec. The soak zone then occurs from 100 to 180°C and should last for 90 to 120 seconds. Finally the temperature raises to 230°C~245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.

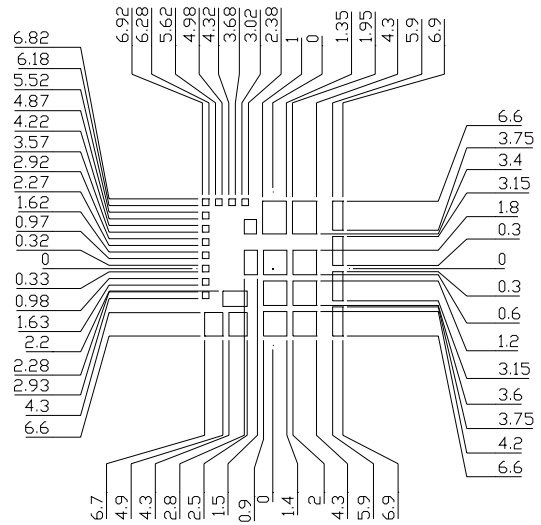


Figure 23. Stencil Pattern with Square Pads

PACKAGE DESCRIPTION

Recommended Reflow Profile
OL213 Solder Paste: SAC305(Sn96.5/Ag3.0/Cu0.5) Alloy, mp. 216~219°C

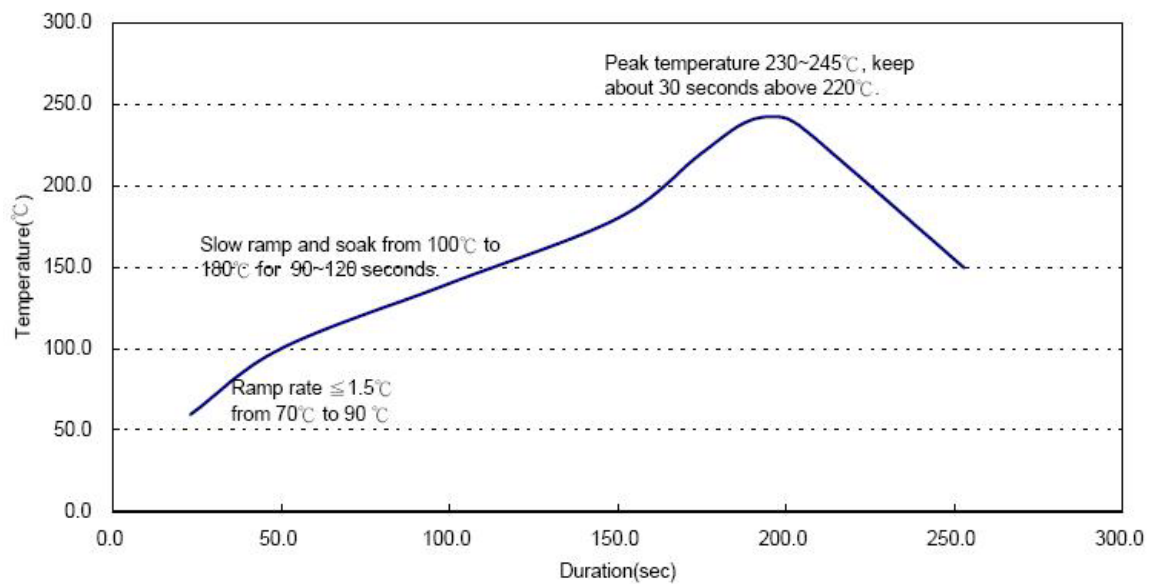


Figure 24. Recommended Reflow Profile

Additional Notes

Storage and Handling Precautions

This document is to provide customers with information related to storage and handling precautions of POL module. Improper packing and handling of POL module tends to trap moisture into the devices and causes damage during soldering process. The following precautions must be taken to protect the module.

Moisture Barrier Bag

Although POL module is a kind of package devices and its inner components are all protected by the package compounds, it is still probably damaged during soldering process if moisture is absorbed into package. The modules firstly are packed in a reel, then an aluminum moisture barrier bag is used to pack the reel in order to prevent moisture absorption. Silica gel is put into the aluminum moisture barrier bag as absorbent material.

Storage

The POL module pack storage follows the JEDEC J-STD-033B01 and J-STD-020C standards. Table 2 is the floor life and moisture sensitive level defined by JEDEC. POL module is classified into level 3. The floor life starts to estimate while the aluminum moisture barrier bag is opened. Under the storage situation of 30°C/60% RH, the device can keep 168 hours floor life after the pack opened. If there are unused POL modules remained, they should be resealed in original moisture barrier bag as soon as possible. However, in case of the modules' floor life

exceeding the defined time period, baking process will be necessary to dehumidify. The method is to bake the module in an oven at 120°C /1% RH (e.g. hot nitrogen gas atmosphere) for 48 hours.

Handling/Others

To protect the POL module and to make sure its normal use, something should be noticed as below.

1. Please handle the POL module carefully to avoid unnecessary mechanism stress on it. Improperly external stress may cause unexpected damage.
2. The ESD wrist strap, ESD shoe strap or anti-electrostatic glove are recommended to be used whenever handling POL module.
3. If cleaning the module is necessary, please use alcohol or IPA solution to clean it under normal room temperature. Avoid the use of unspecified solvent.

Level	Floor Life (out of bag) at factory ambient $\leq 30^{\circ}\text{C}/60\% \text{RH}$ or as stated
1	Unlimited at $\leq 30^{\circ}\text{C}/85\% \text{RH}$
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.

Table 2. Moisture Classification Level and Floor Life